Using the ISL6420A PWM Controller Evaluation Board

Application Note | September 15, 2006 | AN1179.1

Advanced Single Synchronous Buck Pulse-Width Modulation (PWM) Controller

The ISL6420A simplifies the implementation of a complete control and protection scheme for a high-performance DC/DC buck converter. It is designed to drive N-channel MOSFETs in a synchronous rectified buck topology. The control, output adjustment, monitoring and protection functions into a single package.

The ISL6420A provides simple, single feedback loop, voltage mode control with fast transient response. The output voltage of the converter can be precisely regulated to as low as 0.6V, with a maximum tolerance of ±1.0% over temperature and line voltage variations.

The operating frequency is fully adjustable from 100kHz to 1.4MHz. High frequency operation offers cost and space savings.

The error amplifier features a 15MHz gain-bandwidth product and 6V/µs slew rate that enables high converter bandwidth for fast transient response. The resulting PWM duty cycle ranges from 0% to 100%. The capacitor value from the ENSS pin to ground sets the time duration for the PWM soft-start. Pulling the ENSS pin LOW disables the controller.

The ISL6420A monitors the output voltage and generates a PGOOD (power good) signal when soft-start is complete and the output is within regulation. A built-in overvoltage protection circuit prevents the output voltage from going above typically 115% of the set point. Protection from overcurrent conditions is provided by monitoring the $r_{DS(ON)}$ of the upper MOSFET to inhibit the PWM operation appropriately. This approach simplifies the implementation and improves efficiency by eliminating the need for a current sensing resistor. The IC also features voltage margining for networking DC/DC converter applications.

ISL6420A Reference Design

The ISL6420A evaluation boards illustrates the operation of the IC in an embedded application. Two versions of the evaluation board, based on the package type, are listed in Table 1. Both are configured for an output voltage of 3.3V and 10A maximum load.

TABLE 1.

BOARD NAME	IC	PACKAGE
ISL6420AEVAL1Z	ISL6420AIAZ	20 Ld QSSOP
ISL6420AEVAL3Z	ISL6420AIRZ	20 Ld QFN

Quick Start Evaluation

The evaluation board is shipped “ready to use” right from the box. Both boards have been optimized for a 12V input from a standard power supply but can accept a range from 4.5V to 5.5V or 5.5V to 28V as desired. Standoff terminals have been provided in order to connect the input source and the load.

Recommended Test Equipment

To test the functionality of the ISL6420A, the following equipment is recommended:

- An adjustable 30V, 8A capable bench power supply
- An electronic load
- Four channel oscilloscope with probes
- Precision digital multimeter

Power and Load Connections

JUMPER SETTING FOR ISL6420AEVAL1Z

Connect JP1 pin 1 to pin 2 for 5.5V to 28V operation and JP1 pin 2 to pin 3 for a 4.5V to 5.5V operation. JP2 and JP3, when shorted with a jumper, pull the GPIO2 and GPIO1 pins to GND. With the jumpers removed, GPIO2 and GPIO1 will be floating.

CAUTION: When JP1 pin 2 to pin 3 are connected, applying voltages >6V can damage the IC.

JUMPER SETTING FOR ISL6420AEVAL3Z

Connect power supply to the VIN terminal for a 5.5V to 28V operation and source to both VIN and +5V terminals for a 4.5V to 5.5V operation. JP2 and JP3, when shorted with a jumper, pull the GPIO2 and GPIO1 pins to GND. With the jumpers removed, GPIO2 and GPIO1 will be floating.

CAUTION: Ensure that the +5V terminal is not connected to when applying voltages >6V. This can damage the IC.

Input Voltage - The evaluation board is optimized for an input supply of 12V, however, the input supply based on the connection can range from 4.5V to 5.5V or 5.5V to 28V. In the use of the 5.5V to 28V range, an additional 5V source is not required.

If using an input supply ranging from 5.5V to 28V, the VIN post (P1) is connected to the drain of the upper MOSFET and the VIN pin of the IC. The chip is biased by the 5V output (VCC5, post P5) of the internal LDO.

When using a 5V ±10% input supply, connect the power supply to the VIN (P1) post and the VCC5 (P5) post. This will disable the internal LDO and the chip will be powered by the input power supply.

For quick start evaluation, adjust the power supply to the desired VIN. With the power supply turned off, connect the positive lead to the VIN post (P1) and the ground lead to the GND post (P2).

Output Voltage Loading and Monitoring - Connect the positive lead of the electronic load and the positive lead of a digital multimeter to the VOUT post (P3) and the ground lead to the GND post (P4). You can use the scope probe terminal (SC1) to monitor VOUT with an oscilloscope.

Start-up

The Power On Reset (POR) function initiates the soft-start sequence. An internal 10µA current source charges an external capacitor connected to the ENSS (P9) pin from 0V to 3.3V. When the ENSS pin reaches 1V, the error amplifier reference voltage ramps from 0V to 0.6V following the slope of the ENSS pin voltage.

There are two distinct start-up methods for the ISL6420A. The first method is invoked through the application of power to the IC. The soft-start feature allows for a controlled turn-on of the output once the POR threshold of the input voltage has been reached. Figure 1 shows the start-up profile of the regulator in relation to the start-up of the input supply.

V_{IN} = 28V, V_{OUT} = 3.3V, I_{OUT} = 10A

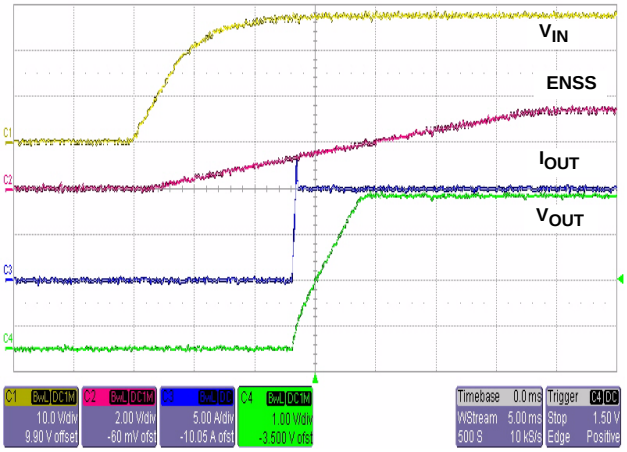


FIGURE 1. SOFT-START

The second method of start-up is through the use of the enable feature. Holding the ENSS (P9) pin on the ISL6420A below 1V will disable the regulator by forcing both the upper and lower MOSFETs off. Releasing the pin allows the regulator to start-up.

Shutdown

If the ENSS pin is pulled down and held below 1V, the regulator will be turned off. Figure 2 shows the shutdown profile of the regulator with the ENSS pin pulled low. Figure 3 shows the shutdown of the regulator when powering down the input supply.

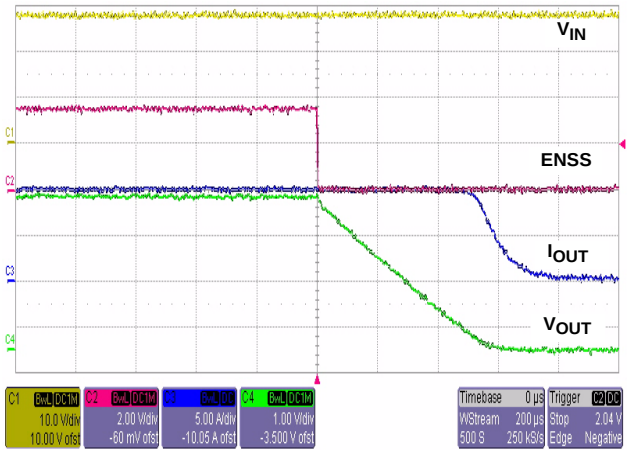


FIGURE 2. SHUTDOWN USING ENSS

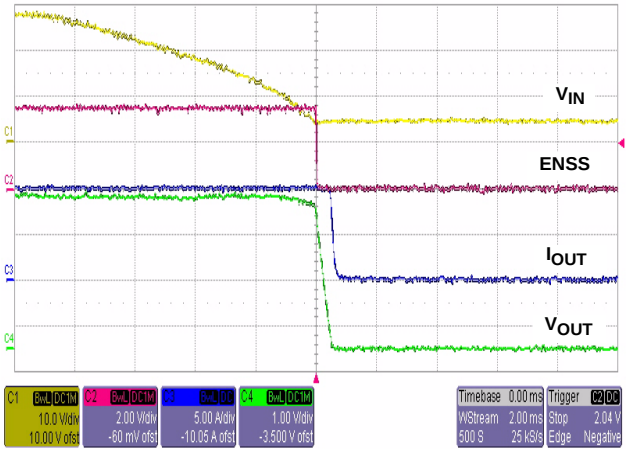


FIGURE 3. POWER-DOWN OF V_{IN}

Output Performance

Switching Frequency

The evaluation board has a 0Ω resistor R9 connecting RT to VCC5 setting the free-running switching frequency to 300kHz. The frequency can be programmed to a different value by removing R9 and populating the R4 location with a resistor value based on the desired frequency.

Output Ripple

Figure 4 shows the ripple voltage on the output of the regulator at the free running 300kHz frequency.

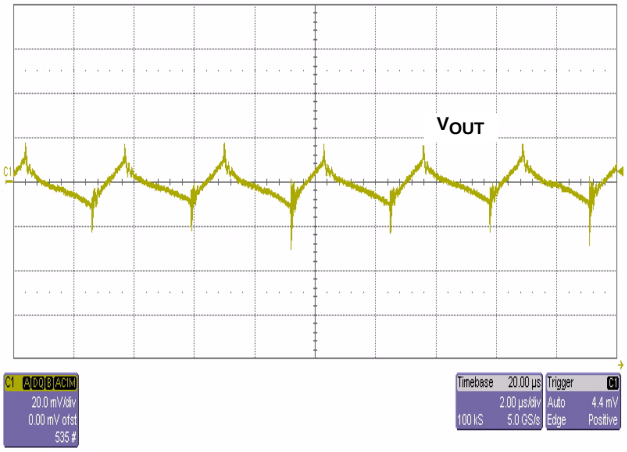


FIGURE 4. OUTPUT RIPPLE

Efficiency

ISL6420A-based regulators enable the design of highly efficient systems. The efficiency of the evaluation board using a 12V and a 28V input supply is shown in Figure 5.

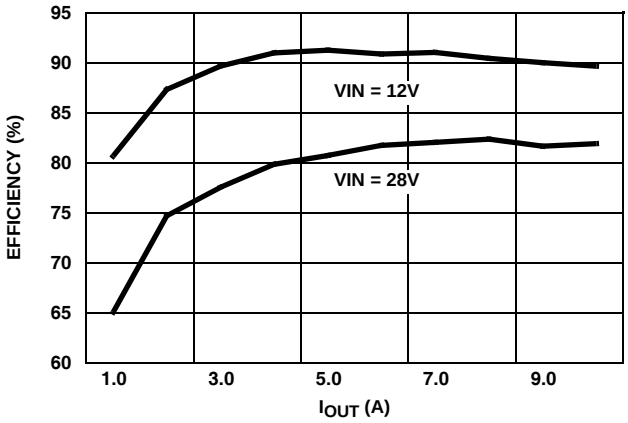


FIGURE 5. EVALUATION BOARD EFFICIENCY (V_{OUT} = 3.3V)

Power Good

PGOOD will be true (open drain) when the FB pin voltage is within ±10% of the reference voltage and the soft-start sequence is complete, i.e., once the soft-start capacitor is finished charging. The status of PGOOD can be monitored at the PGOOD test point (TP1).

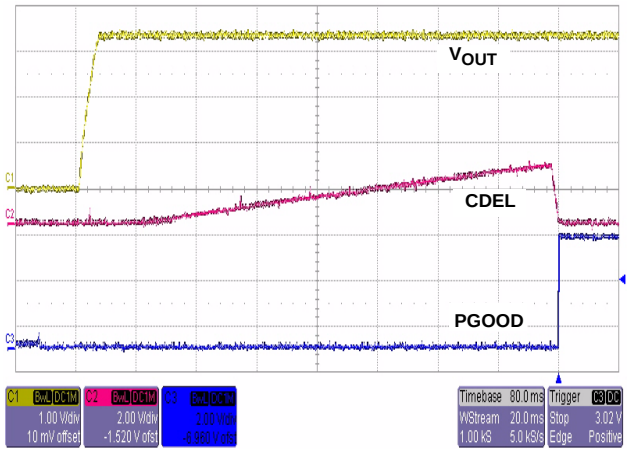


FIGURE 6. PGOOD

Overcurrent Protection

The overcurrent function cycles the soft-start function in a hiccup mode to provide fault protection. Figure 7 shows the overcurrent hiccup mode.

The overcurrent function protects the converter from a shorted output by using the upper MOSFET's $r_{DS(ON)}$ to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor.

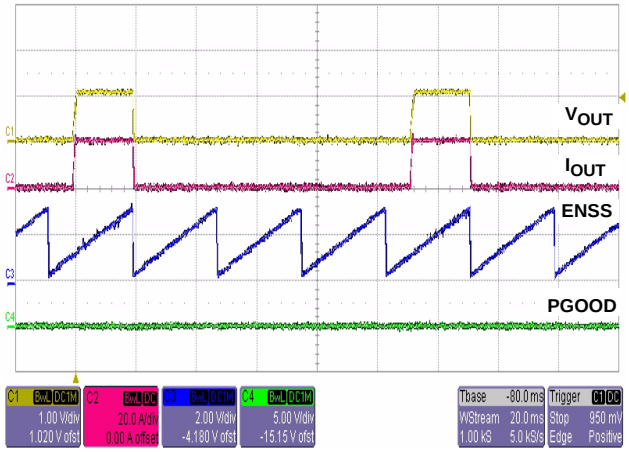


FIGURE 7. OVERCURRENT HICCUP MODE

A resistor, R_{OCSET} (R8), programs the overcurrent trip level. The PHASE node voltage is compared to the voltage on the OCSET pin while the upper FET is on. A current (100µA typically) is pulled from the OCSET pin to establish this voltage across an external resistor. If PHASE is lower than OCSET, while the upper FET is on, then an overcurrent condition is detected for that clock cycle. The pulse is immediately terminated, and a counter is incremented. If an overcurrent condition is detected for 8 consecutive clock cycles, and the circuit is not in soft-start, the ISL6420A enters into hiccup mode. During hiccup, the external

capacitor on the ENSS pin is discharged and soft-start is initiated. During soft-start, pulse termination limiting is enabled, but the 8-cycle hiccup counter is held in reset until soft-start is completed.

The overcurrent function will trip at a peak inductor current (I_{PEAK}) determined by,

$$I_{PEAK} = \frac{I_{OCSET} \bullet R_{OCSET}}{R_{DS(ON)}}$$

where I_{OCSET} is the internal OCSET current source.

The OC trip point varies mainly due to the MOSFET's $r_{DS(ON)}$ variations. To avoid overcurrent tripping in the normal operating load range, calculate the R_{OCSET} resistor from the equation above using:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature
2. The minimum I_{OCSET} from the specification table

Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + (\Delta I)/2$,

where ΔI is the output inductor ripple current. A small ceramic capacitor should be placed in parallel with R_{OCSET} to smooth the voltage across R_{OCSET} in the presence of switching noise on the input voltage.

The overcurrent trip point on the evaluation board has been set to 16A. Figure 7 shows the overcurrent hiccup mode.

Transient Performance

Figure 8 shows the response of the output when subjected to transient loading from 10mA to 10A.

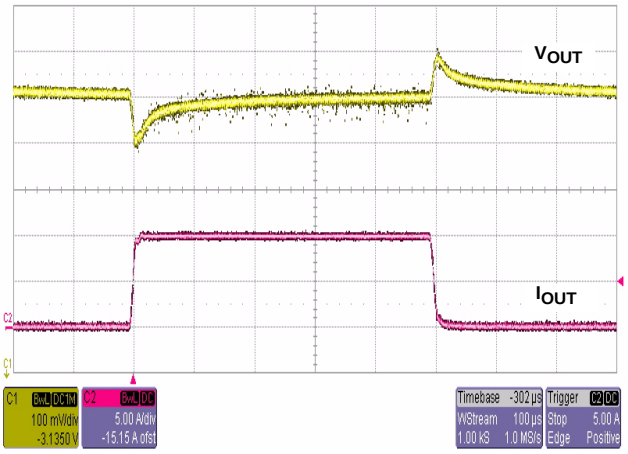


FIGURE 8. TRANSIENT RESPONSE

Voltage Margining

Voltage margining mode is enabled by connecting a margining set resistor (R6) from the VMSET pin to ground. This resistor to ground will set a current, which is switched to the FB pin. The current will be equal to 2.468V divided by the value of the external resistor tied to the VMSET pin.

The GPIO1 (P8) and GPIO2 (P7) pins control the current switching as per Table 2. The power supply output increases when GPIO2 is HIGH and decreases when GPIO1 is HIGH. Using a jumper to short the pins of JP2 and JP3 will pull GPIO2 and GPIO1 LOW, respectively. Remove one of the jumpers to pull GPIO1 or GPIO2 HIGH for voltage margining. The amount that the output voltage of the power supply changes with voltage margining will be equal to 2.468V times the ratio of the external feedback resistor (R2) and the external resistor tied to VMSET (R6).

TABLE 2.

GPIO1	GPIO2	V_{OUT}
L	L	No Change
L	H	+ Delta V_{OUT}
H	L	- Delta V_{OUT}
H	H	Ignored

The evaluation board has a 330kΩ VMSET resistor (R6) setting a current:

IVM = 2.468V/330kΩ = 7.48µA

and

V(delta) = 7.48µA*20.5kΩ = 0.153V

Figure 9 shows the output voltage in voltage margining mode for various VMSET resistor values.

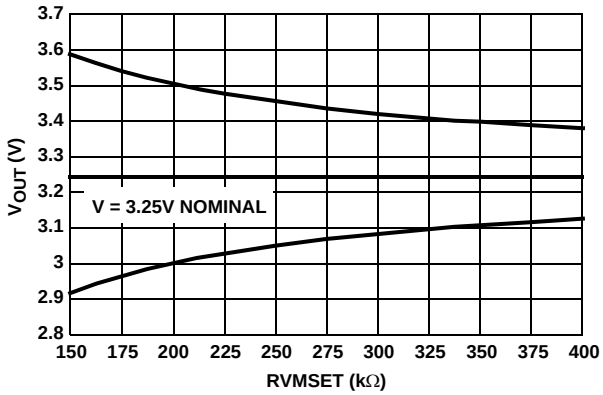


FIGURE 9. CHANGE IN OUTPUT VOLTAGE FOR VARIOUS RESISTORS

The slew time of the current is set by an external capacitor (C13) on the CDEL pin, which is charged and discharged with a 100µA current source. The change in voltage on the capacitor is 2.5V. This same capacitor is also used to set the PGOOD rise delay. When PGOOD is low, the internal PGOOD circuitry uses the capacitor and when PGOOD is high the voltage margining circuit uses the capacitor. The slew time for voltage margining can be in the range of 300µs to 2.5ms. The CDEL capacitor on the evaluation board is 0.1µF leading to a voltage margining slew rate of 2.5ms.

Figures 10 and 11 show negative and positive voltage margining with a CDEL capacitor of 0.1µF.

V_{IN} = 12V, V_{OUT} = 3.3V, NO LOAD

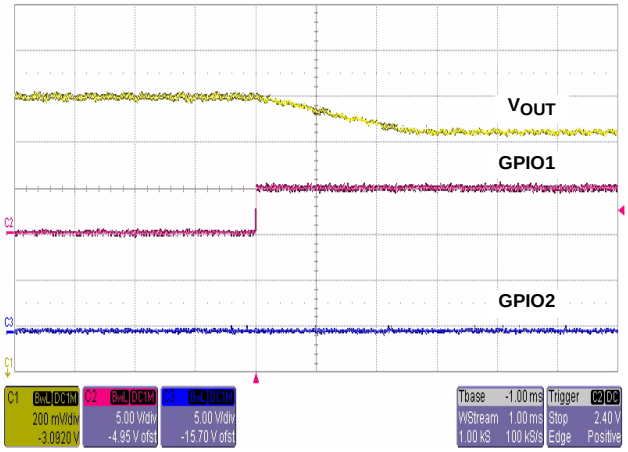


FIGURE 10. NEGATIVE VOLTAGE MARGINING SLEW TIME

V_{IN} = 12V, V_{OUT} = 3.3V, NO LOAD

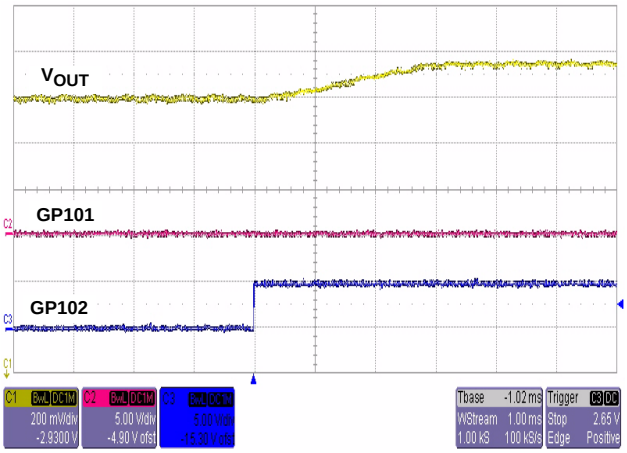


FIGURE 11. POSITIVE VOLTAGE MARGINING SLEW TIME

Layout Guidelines

DC to DC converter layout is extremely important to obtain the desired attenuation to the EMI frequencies. Poor layout practice can cause conducted emissions to actually couple around the filter components directly into the input conductors or cause radiated emissions. The copper traces of power input and output and high current paths must be sized according to the RMS current passing through them. Keep the high current loops small and the path defined. Use single point grounding. Capacitor lead length must be minimized as much as possible to reduce ESL. This includes the traces on the PC board leading up to the capacitor pads. Based on the layout, voltage transients may reduce the level of the acceptable max VIN when operating close to 28V. In this case, one can consider the use of snubbers or reduce the max VIN. Use of a GND plane in a multilayered board is preferred.

Conclusion

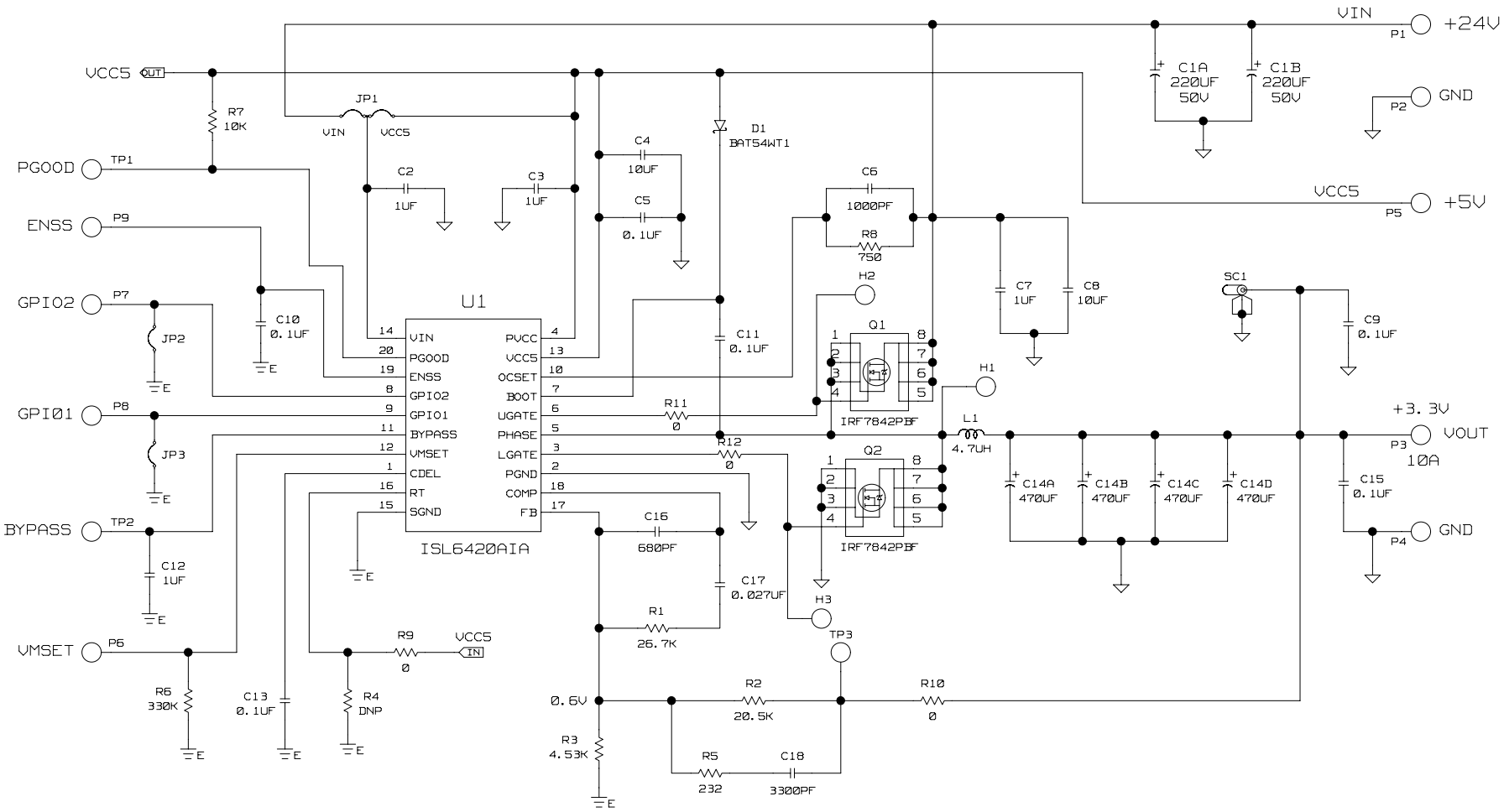
The ISL6420A is a versatile PWM controller. The small footprint and the numerous features enables the implementation of compact and highly efficient regulators, delivering low voltage power solutions.

References

For Intersil documents available on the web, see http://www.intersil.com/

[1] *ISL6420A Data Sheet,* Intersil Corporation, File No. FN9073.

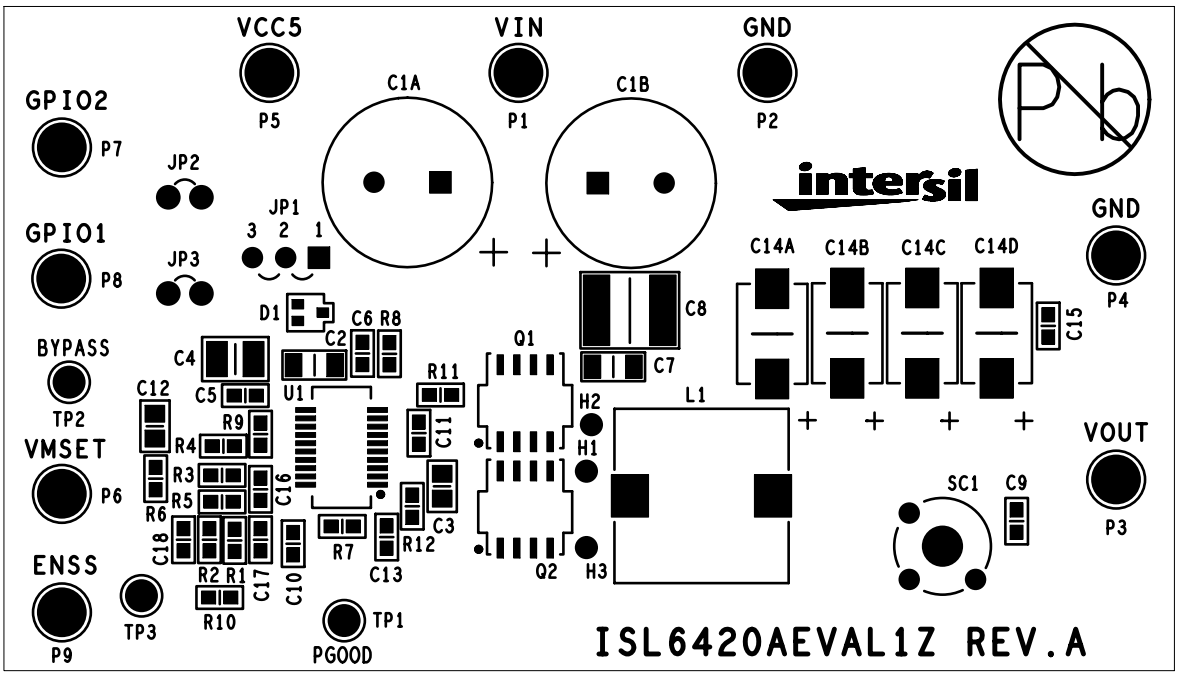
ISL6420AEVAL1Z Schematic



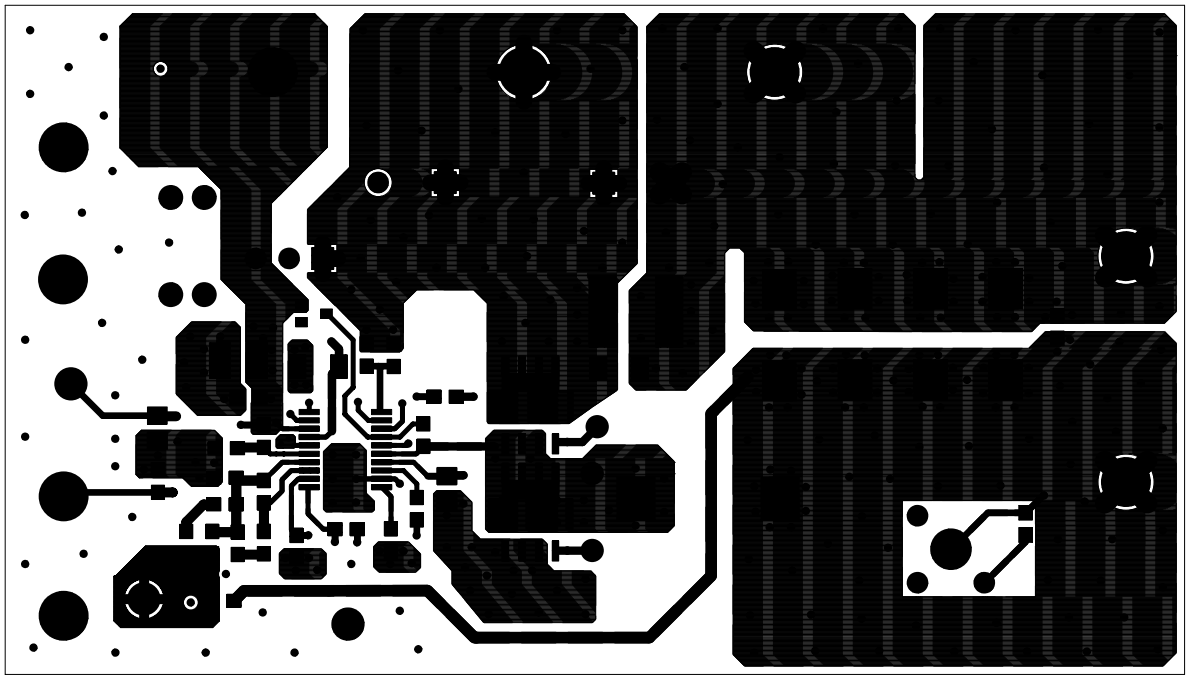
ISL6420AEVAL1Z Rev. A Bill of Materials

ID	REFERENCE	QTY	PART NUMBER	PART TYPE	DESCRIPTION	PACKAGE	VENDOR
1	U1	1	ISL6420AIAZ	IC, Linear	IC, Single PWM Controller	20 Ld QSOP	Intersil
2	Q1, Q2	2	IRF7842PBF	MOSFET, Single	N-channel, 40V, 18A	SO-8	International Rectifier
3	D1	1	BAT54WT-7-F	Diode, Schottky	30V, 200mA	SOT-323	Diode Inc.
4	L1	1	IHLP-5050CEEB4R7M01	Inductor	4.7µH, 20%, 24A	SMD	Vishay
CAPACITORS							
5	C1A, C1B	2	EEUFC1H221S	Capacitor, Alum. Elec.	220µF, 20%, 50V, 1150mA	12.5 X 15	Panasonic
6	C2, C7	2	C3216X7R1H105K	Capacitor, Ceramic, X7R	1.0µF, 10%, 50V	SM_1206	TDK/Generic
7	C3, C12	2	C2012X7R1E105K	Capacitor, Ceramic, X7R	1.0µF, 10%, 25V	SM_0805	TDK/Generic
8	C4	1	C3225X7R1E106M	Capacitor, Ceramic, X7R	10µF, 20%, 25V	SM_1210	TDK/Generic
9	C5, C9, C10, C11, C13, C15	6	C1608X7R1E104K	Capacitor, Ceramic, X7R	0.1µF, 10%, 25V	SM_0603	TDK/Generic
10	C6	1	C1608X7R1H102K	Capacitor, Ceramic, X7R	1000pF, 10%, 50V	SM_0603	TDK/Generic
11	C8	1	C5750X7R1H106M	Capacitor, Ceramic, X7R	10µF, 20%, 50V	SM_2220	TDK/Generic
12	C14A, C14B, C14C, C14D	4	6TPB470M	Capacitor, POSCAP	470µF, 20%, 6.3V, 0.035Ω	Case D4	SANYO
13	C16	1	C1608COG1H681JT	Capacitor, Ceramic, X7R	680pF, 10%, 25V	SM_0603	TDK/Generic
14	C17	1	C1608X7R1E273K	Capacitor, Ceramic, X7R	0.027µF, 10%, 25V	SM_0603	TDK/Generic
15	C18	1	C1608X7R1E332K	Capacitor, Ceramic, X7R	3300pF, 10%, 25V	SM_0603	TDK/Generic
RESISTORS							
16	R1	1		Resistor, Film	26.7kΩ, 1%, 1/16W	SM_0603	Panasonic/Generic
17	R2	1		Resistor, Film	20.5kΩ, 1%, 1/16W	SM_0603	Panasonic/Generic
18	R3	1		Resistor, Film	4.53kΩ, 1%, 1/16W	SM_0603	Panasonic/Generic
19	R4	1	Do Not Populate	Resistor, Film		SM_0603	Panasonic/Generic
20	R5	1		Resistor, Film	232Ω, 1%, 1/16W	SM_0603	Panasonic/Generic
21	R6	1		Resistor, Film	330kΩ, 1%, 1/16W	SM_0603	Panasonic/Generic
22	R7	1		Resistor, Film	10kΩ,1%,1/16W	SM_0603	Panasonic/Generic
23	R8	1		Resistor, Film	750Ω, 1%, 1/16W	SM_0603	Panasonic/Generic
24	R9, R10, R11, R12	4		Resistor, Film	0Ω, 1%, 1/16W	SM_0603	Panasonic/Generic
OTHERS							
25	SC1	1	Do Not Populate	Terminal, Scope Probe	Terminal, Scope Probe		Tektronix
26	P1 - P9	9	1514-2	Turrett Post	Terminal post, through hole, 1/4 inch	PTH	Johnson
27	TP1, TP2, TP3	3	5002	TEST POINT vertical, white	PC test jack	PTH	Keystone
28	JP1	1	68000-236-1X3	Header	1X3 Break Strip GOLD		
29	JP2, JP3	2	68000-236-1X2	Header	1X2 Break Strip GOLD		
30	JP1, JP2, JP3	3	S9001-ND	Jumper	2 pin jumper		Digikey
31				Bumpers			

ISL6420AEVAL1Z Printed Circuit Board Layers

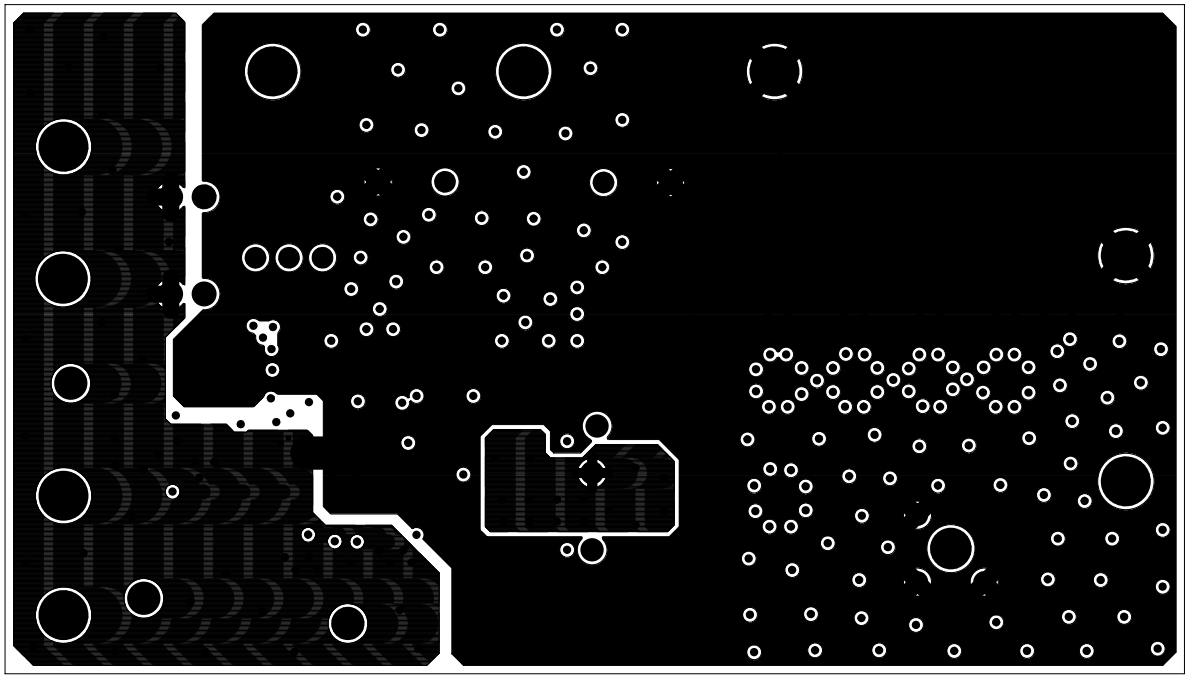


ISL6420AEVAL1Z - TOP LAYER (SILKSCREEN)

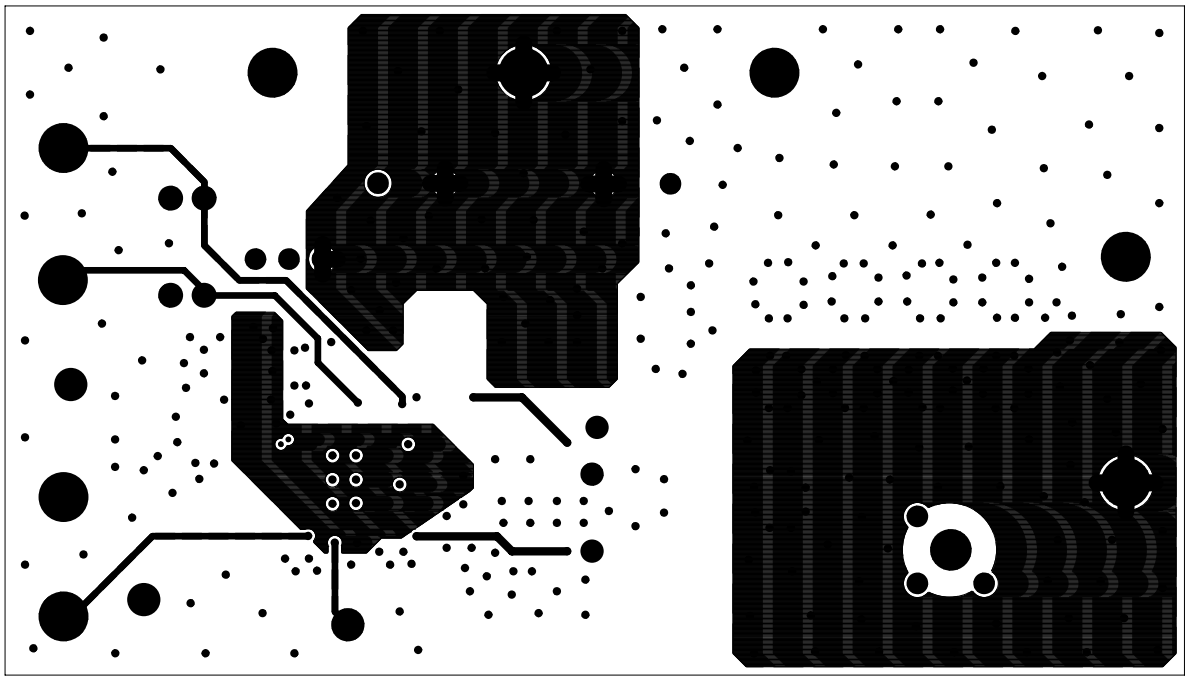


ISL6420AEVAL1Z - TOP LAYER (COMPONENT SIDE)

ISL6420AEVAL1Z Printed Circuit Board Layers (Continued)

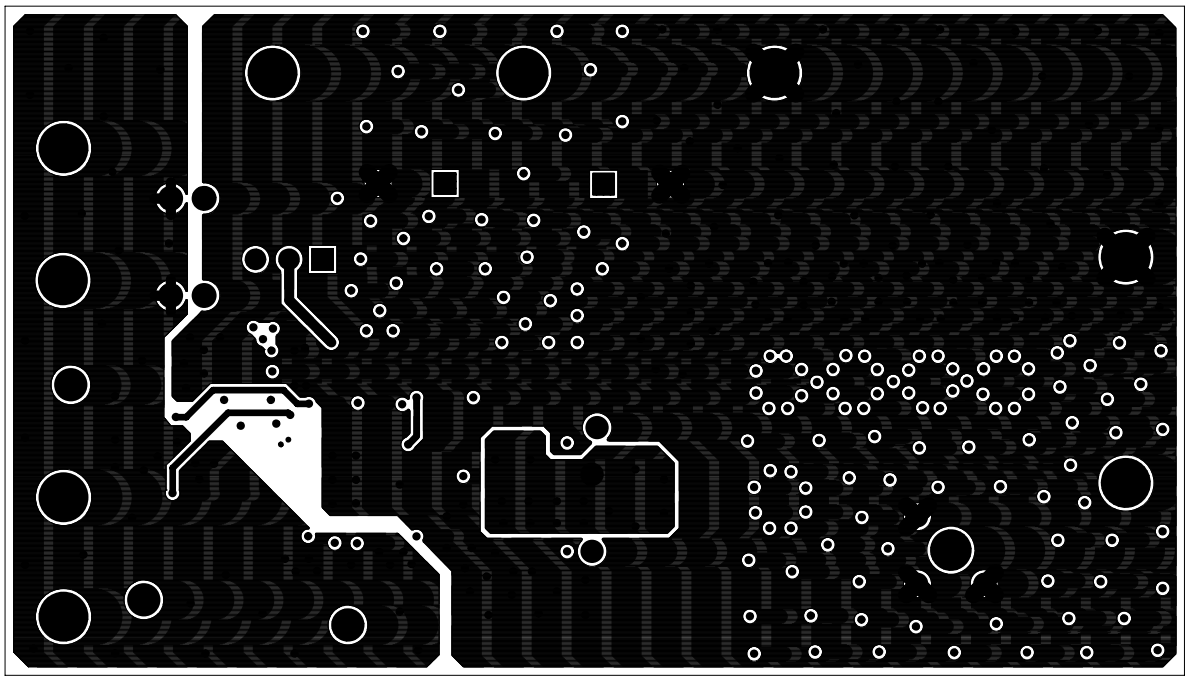


ISL6420AEVAL1Z - LAYER 2

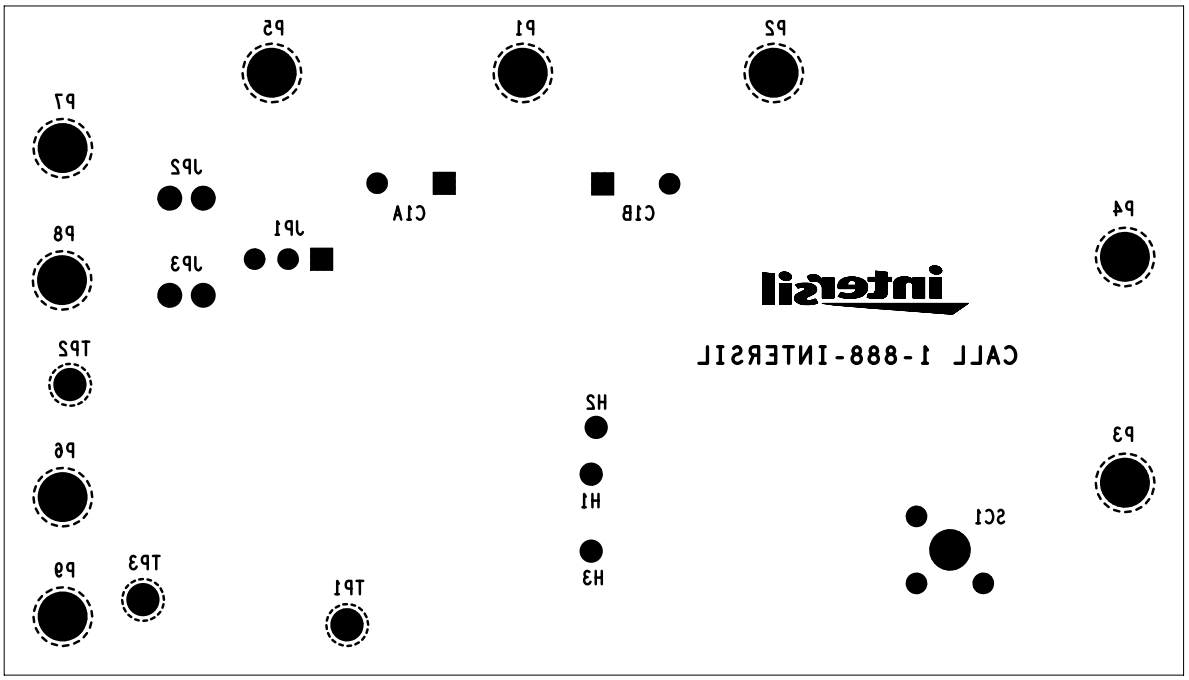


ISL6420AEVAL1Z - LAYER 3

ISL6420AEVAL1Z Printed Circuit Board Layers (Continued)

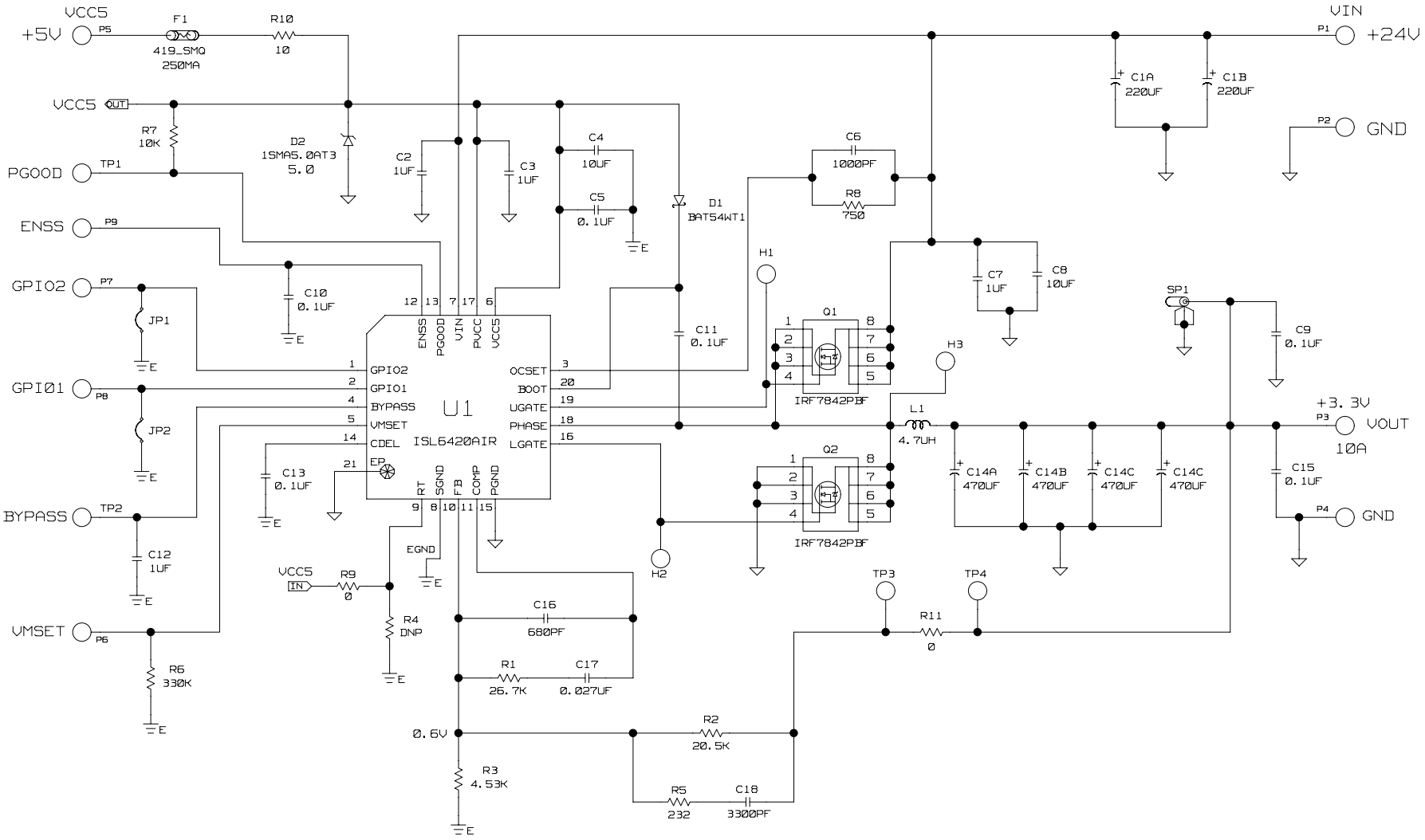


ISL6420AEVAL1Z - BOTTOM LAYER (SOLDER SIDE)



ISL6420AEVAL1Z - BOTTOM LAYER (SILKSCREEN)

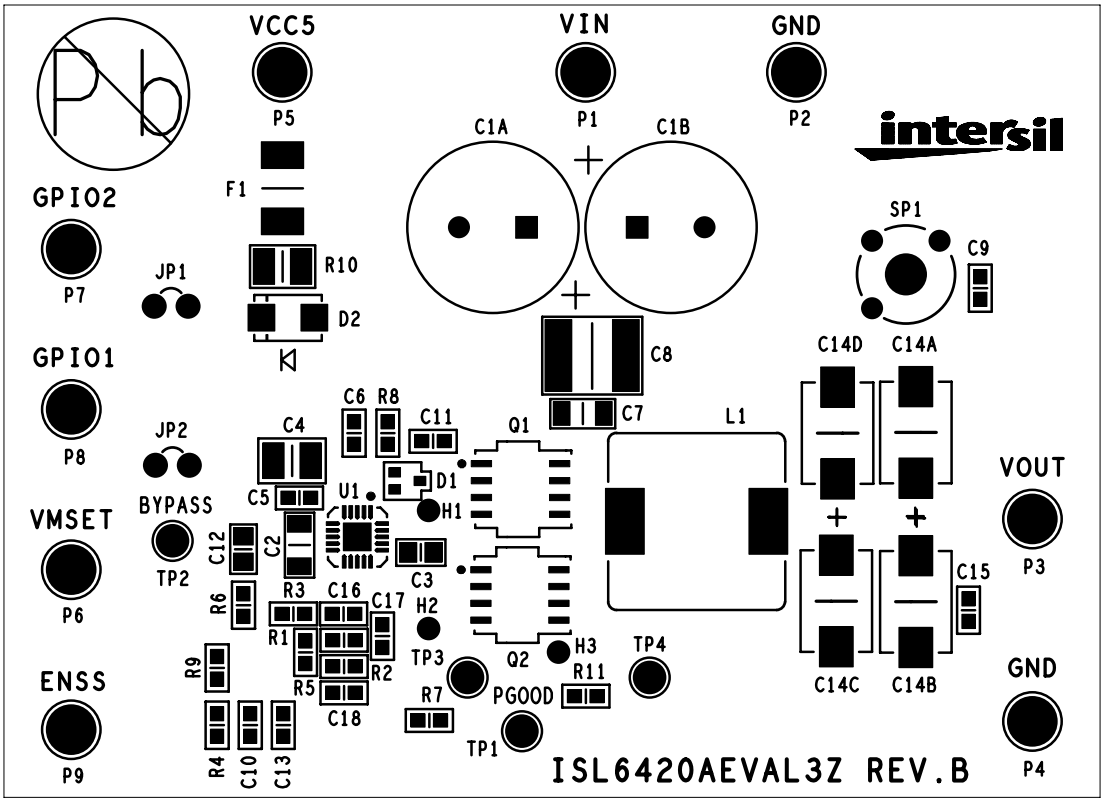
ISL6420AEVAL3Z Schematic



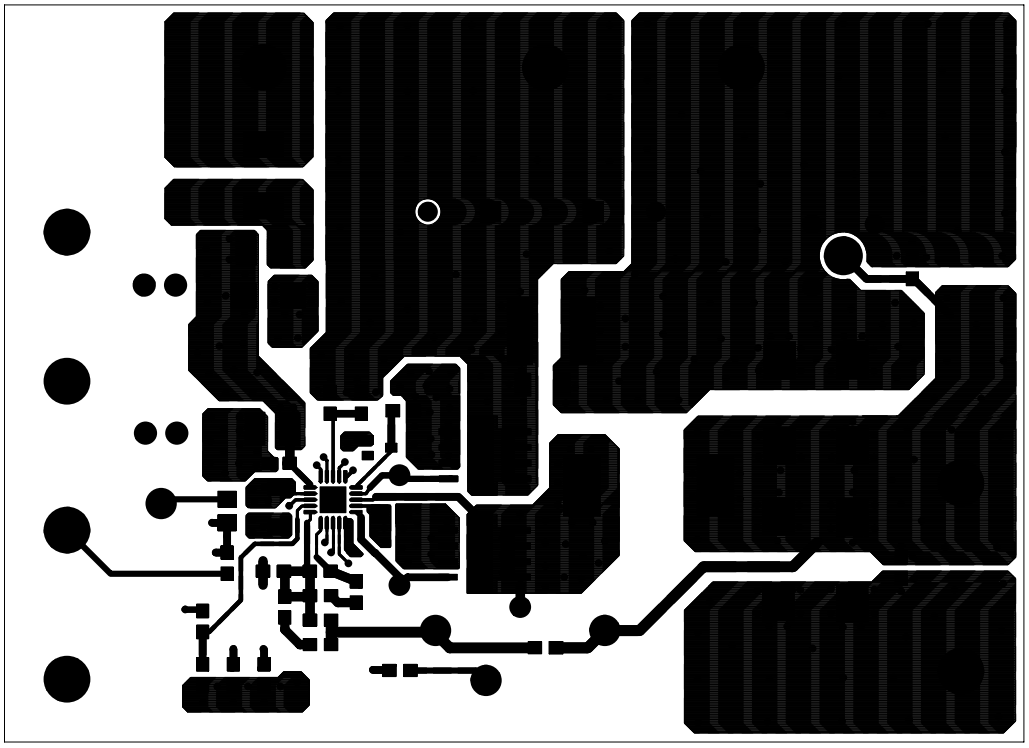
ISL6420AEVAL3Z Rev. B Bill of Materials

ID	REFERENCE	QTY	PART NUMBER	PART TYPE	DESCRIPTION	PACKAGE	VENDOR
1	U1	1	ISL6420AIRZ	IC, Linear	IC, Single PWM Controller	20 Ld QFN	Intersil
2	Q1, Q2	2	IRF7842PBF	MOSFET, Single	N-channel, 40V, 18A	SO-8	International Rectifier
3	D1	1	BAT54WT-7-F-T	Diode, Schottky	30V, 200mA	SOT-323	Diode Inc.
4	D2	1	1SMA5.0AT3G	Diode, Voltage Suppressor	6.4V, 400mA	SMA	On Semi
5	L1	1	IHLP-5050CEEB4R7M01	Inductor	4.7µH, 20%, 24A	SMD	Vishay
CAPACITORS							
6	C1A, C1B	2	EEUFC1H221S	Capacitor, Alum. Elec.	220µF, 20%, 50V, 1150mA	Radial	Panasonic
7	C2, C7	2	C3216X7R1H105K	Capacitor, Ceramic, X7R	1.0µF, 10%, 50V	SM_1206	TDK/Generic
8	C3, C12	2	C2012X7R1E105K	Capacitor, Ceramic, X7R	1.0µF, 10%, 25V	SM_0805	TDK/Generic
9	C4	1	C3225X7R1E106M	Capacitor, Ceramic, X7R	10µF, 20%, 25V	SM_1210	TDK/Generic
10	C5, C9, C10, C11, C13, C15	6	C1608X7R1E104K	Capacitor, Ceramic, X7R	0.1µF, 10%, 25V	SM_0603	TDK/Generic
11	C6	1	C1608X7R1H102K	Capacitor, Ceramic, X7R	1000pF, 10%, 50V	SM_0603	TDK/Generic
12	C8	1	C5750X7R1H106M	Capacitor, Ceramic, X7R	10µF, 20%, 50V	SM_2220	TDK/Generic
13	C14A, C14B, C14C, C14D	4	6TPB470M	Capacitor, POSCAP	470µF, 20%, 6.3V, 0.035Ω	Case D4	SANYO
14	C16	1	C1608X7R1E681K	Capacitor, Ceramic, X7R	680pF, 10%, 25V	SM_0603	TDK/Generic
15	C17	1	C1608X7R1E273K	Capacitor, Ceramic, X7R	0.027µF, 10%, 25V	SM_0603	TDK/Generic
16	C18	1	C1608X7R1E332K	Capacitor, Ceramic, X7R	3300pF, 10%, 25V	SM_0603	TDK/Generic
RESISTORS							
17	R1	1		Resistor, Film	26.7kΩ, 1%, 1/16W	SM_0603	TDK/Generic
18	R2	1		Resistor, Film	20.5kΩ, 1%, 1/16W	SM_0603	TDK/Generic
19	R3	1		Resistor, Film	4.53kΩ, 1%, 1/16W	SM_0603	TDK/Generic
20	R4 (DNP)	1	Do Not Populate	Resistor, Film		SM_0603	TDK/Generic
21	R5	1		Resistor, Film	232Ω, 1%, 1/16W	SM_0603	TDK/Generic
22	R6	1		Resistor, Film	330kΩ, 1%, 1/16W	SM_0603	TDK/Generic
23	R7	1		Resistor, Film	10kΩ, 1%,1/16W	SM_0603	TDK/Generic
24	R8	1		Resistor, Film	750Ω, 1%, 1/16W	SM_0603	TDK/Generic
25	R9, R11	2		Resistor, Film	0Ω, 1%, 1/16W	SM_0603	TDK/Generic
26	R10	1		Resistor, Film	10Ω, 5%, 1/4W	SM_1210	TDK/Generic
OTHERS							
27	F1	1	419-0250-000	Fuse	Fuse, 250mA	SMT	Wickmann
28	SP1	1	Do Not Populate	Terminal, Scope Probe	Terminal, Scope Probe		Tektronix
29	P1 - P9	9	1514-2	Turrett Post	Terminal post, through hole, 1/4 inch	PTH	Johnson
30	TP1, TP2, TP3, TP4	4	5002	TEST POINT vertical, white	PC test jack	PTH	Keystone
31	JP1, JP2	2	69190-202	Header	1X2 Break Strip GOLD		BERG/FCI
32	JP1, JP2	2	SPC02SYAN	Jumper	2 pin jumper		SULLINSSULLINS
33				Bumpers			

ISL6420AEVAL3Z Printed Circuit Board Layers

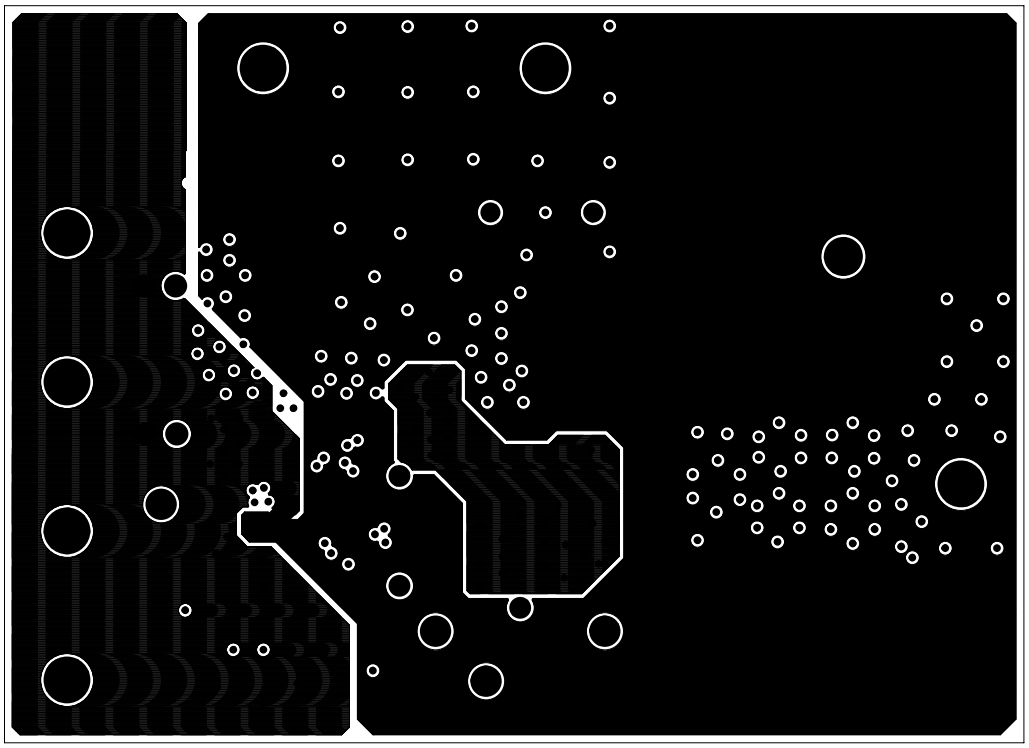


ISL6420AEVAL3Z - TOP LAYER (SILKSCREEN)

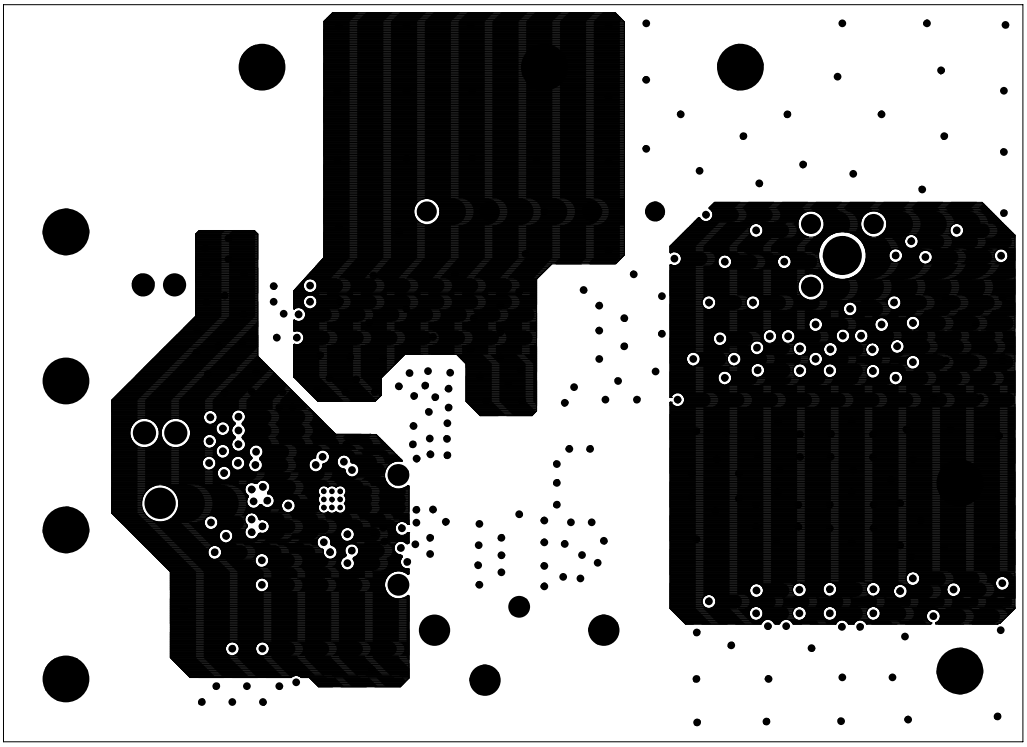


ISL6420AEVAL3Z - TOP LAYER (COMPONENT SIDE)

ISL6420AEVAL3Z Printed Circuit Board Layers (Continued)

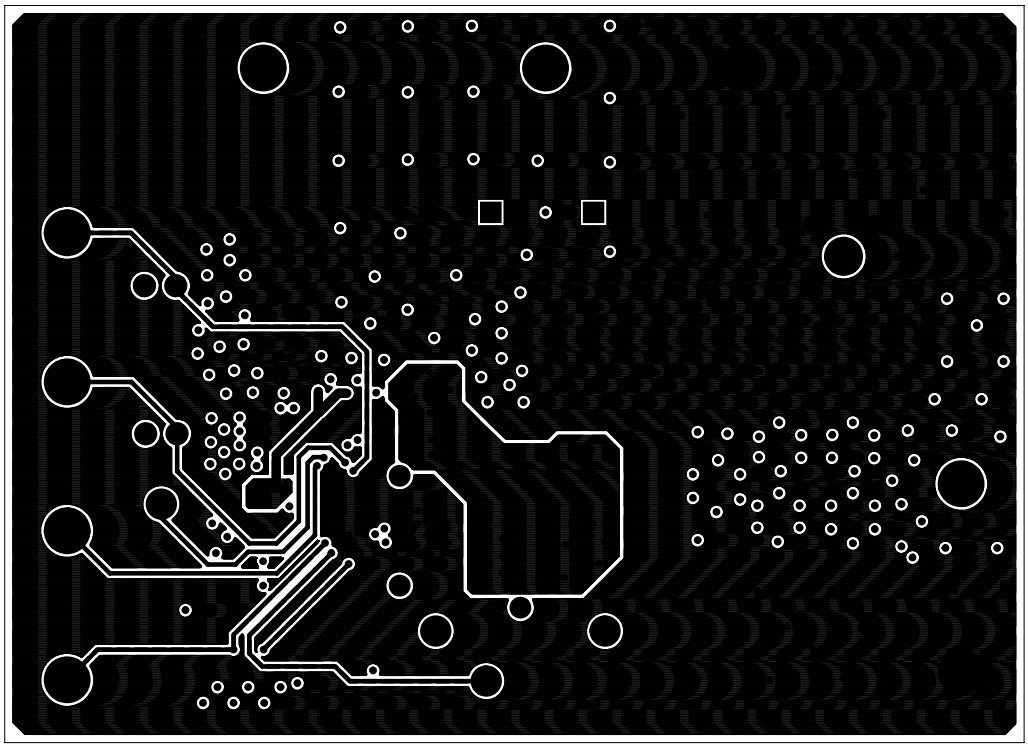


ISL6420AEVAL3Z - LAYER 2

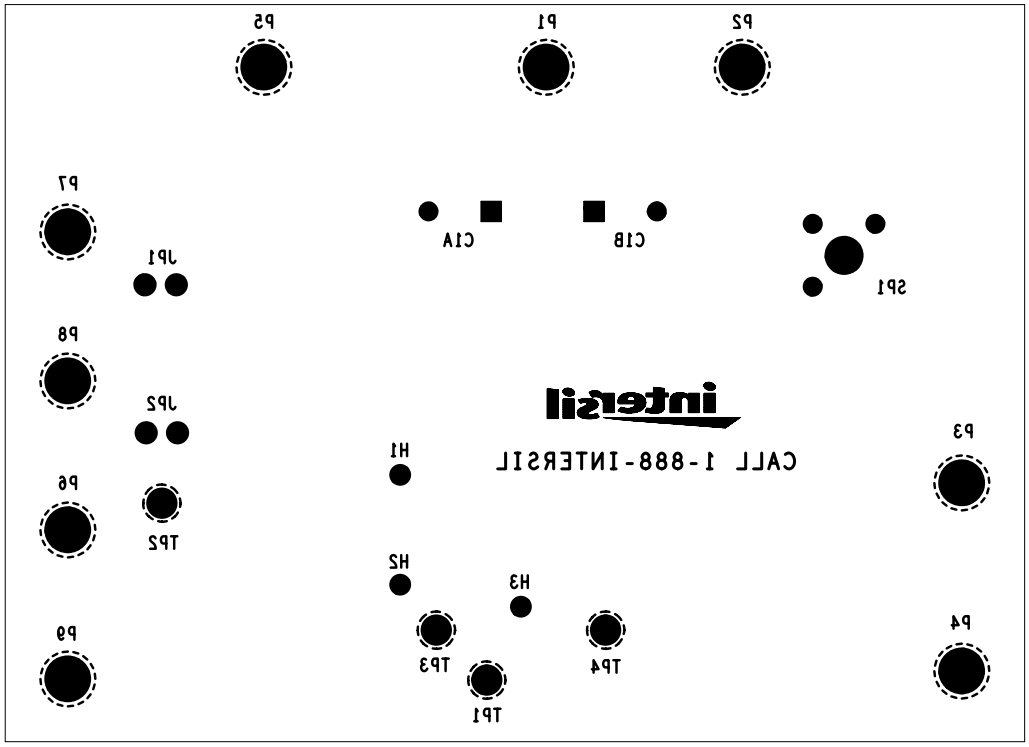


ISL6420AEVAL3Z - LAYER 3

ISL6420AEVAL3Z Printed Circuit Board Layers (Continued)



ISL6420AEVAL3Z - BOTTOM LAYER (SOLDER SIDE)



ISL6420AEVAL3Z - BOTTOM LAYER (SILKSCREEN)